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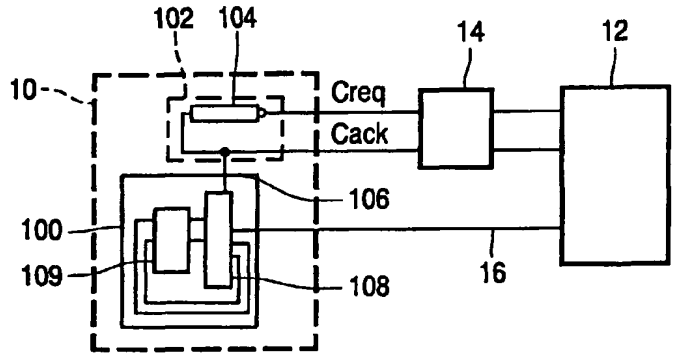
(54) Title: INFORMATION EXCHANGE BETWEEN LOCALLY SYNCHRONOUS CIRCUITS



(57) Abstract: A locally synchronous circuit module has a delay circuit having and input and output coupled to a clock input. The delay circuit provides a delay which when incorporated in a clock oscillator ensures a clock period that is at least as long as needed to transfer information between the storage elements. A handshake circuit is provided for generating handshake signals for timing information transfer between the locally synchronous circuit module and a further circuit. The handshake circuit comprises the delay circuit, so that at least part of the handshake signals during a handshake transaction are timed by travelling through the delay circuit and are applied to the clock input to clock the locally synchronous circuit module.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, COMPENDEX, INSPEC, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	JOEP KESSELS, AD PEETERS, PAUL WIELAGE, SUK-JIN KIM: "Clock Synchronization through Handshake Signalling" PROCEEDINGS OF THE EIGHT INTERNATIONAL SYMPOSIUM ON ASYNCHRONOUS CIRCUITS AND SYSTEMS (ASYNC'02), 8 - 11 April 2002, pages 1-10, XP002259849 the whole document --- -/--	1-10

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

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Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BORMANN D S ET AL: "Asynchronous wrapper for heterogeneous systems" COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, 1997. ICCD '97. PROCEEDINGS., 1997 IEEE INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA 12-15 OCT. 1997, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 12 October 1997 (1997-10-12), pages 307-314, XP010251752 ISBN: 0-8186-8206-X the whole document ---	
A	MUTTERSBACH J ET AL: "Globally-asynchronous locally-synchronous architectures to simplify the design of on-chip systems" ASIC/SOC CONFERENCE, 1999. PROCEEDINGS. TWELFTH ANNUAL IEEE INTERNATIONAL WASHINGTON, DC, USA 15-18 SEPT. 1999, PISCATAWAY, NJ, USA,IEEE, US, 15 September 1999 (1999-09-15), pages 317-321, XP010360322 ISBN: 0-7803-5632-2 the whole document ---	
A	MUTTERSBACH J ET AL: "Practical design of globally-asynchronous locally-synchronous systems" ADVANCED RESEARCH IN ASYNCHRONOUS CIRCUITS AND SYSTEMS, 2000. (ASYNC 2000). PROCEEDINGS. SIXTH INTERNATIONAL SYMPOSIUM ON EILAT, ISRAEL 2-6 APRIL 2000, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 2 April 2000 (2000-04-02), pages 52-59, XP010377337 ISBN: 0-7695-0586-4 the whole document -----	